

Fig. 1

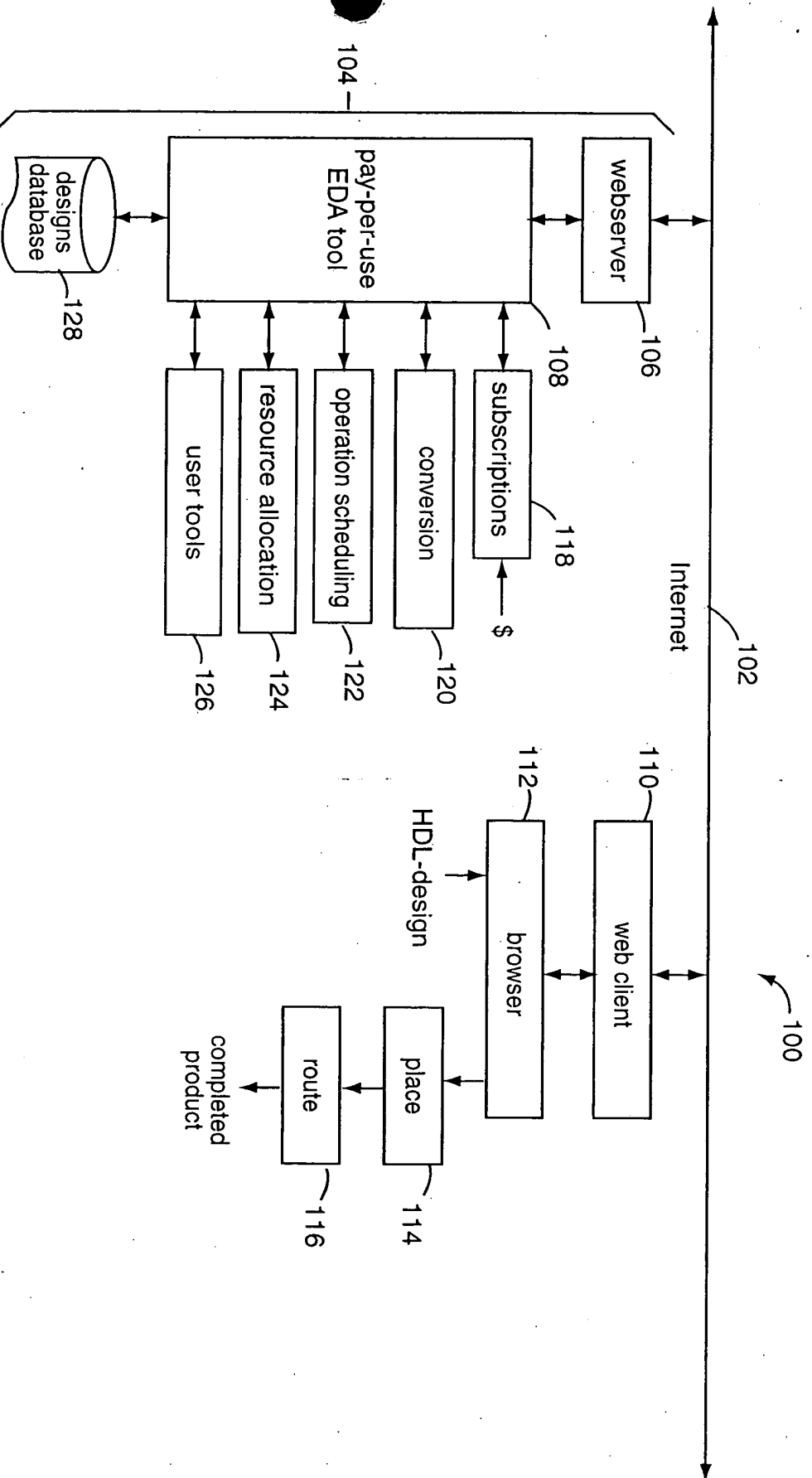


Fig. 2

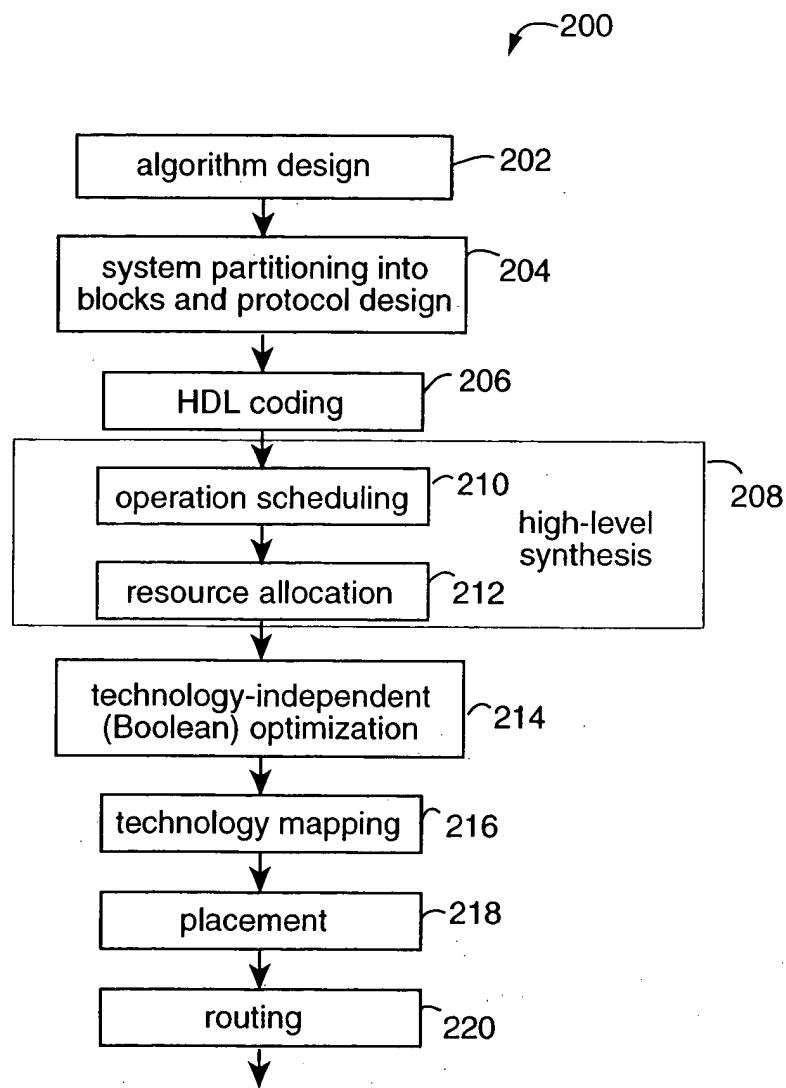


Fig. 3

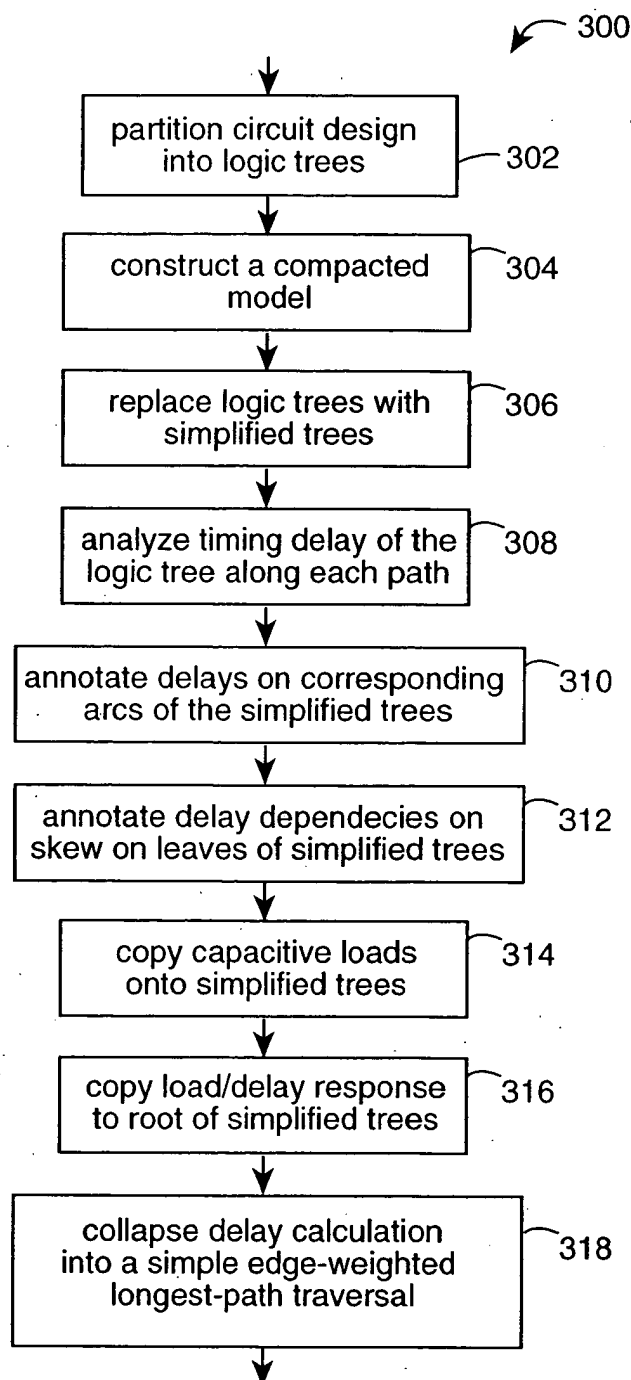


Fig. 4A

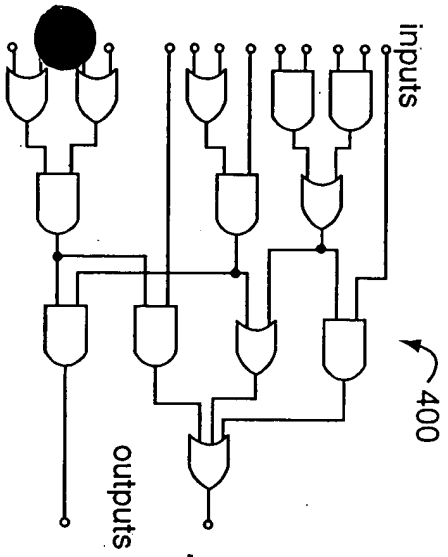


Fig. 4B

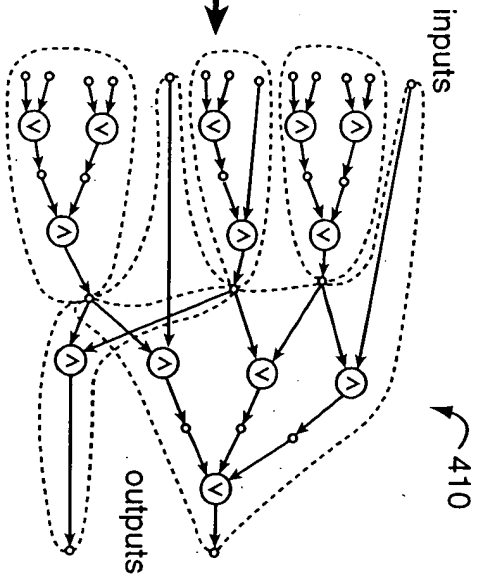
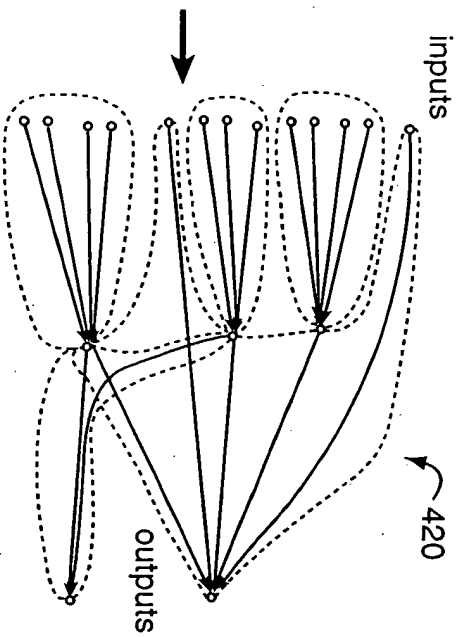
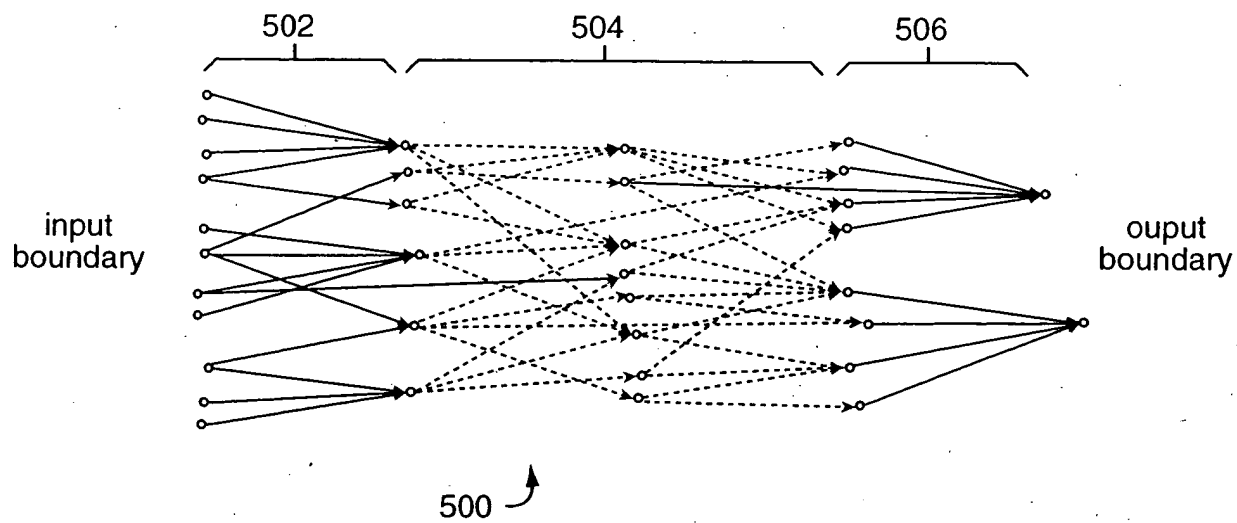


Fig. 4C



005000 535250

Fig. 5



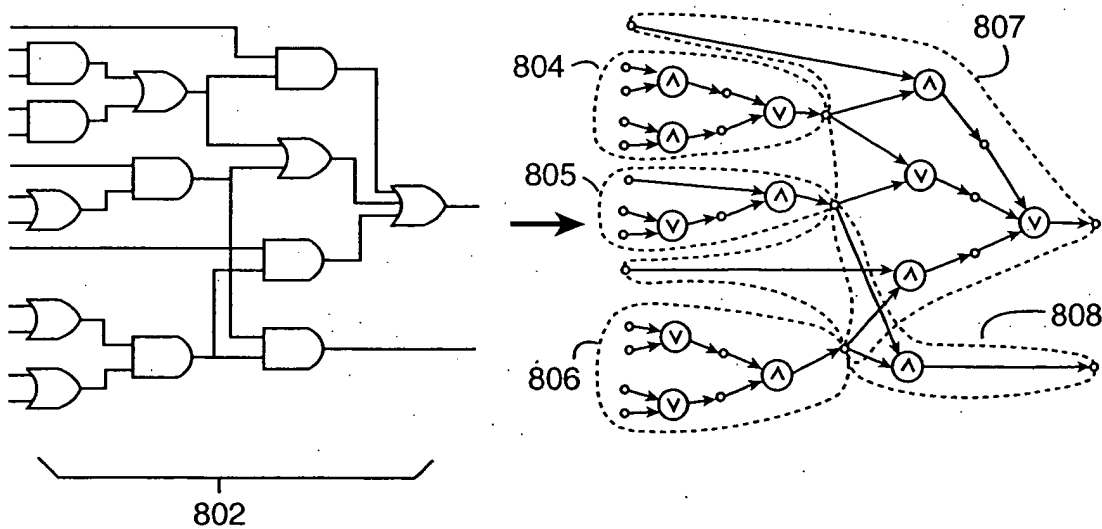
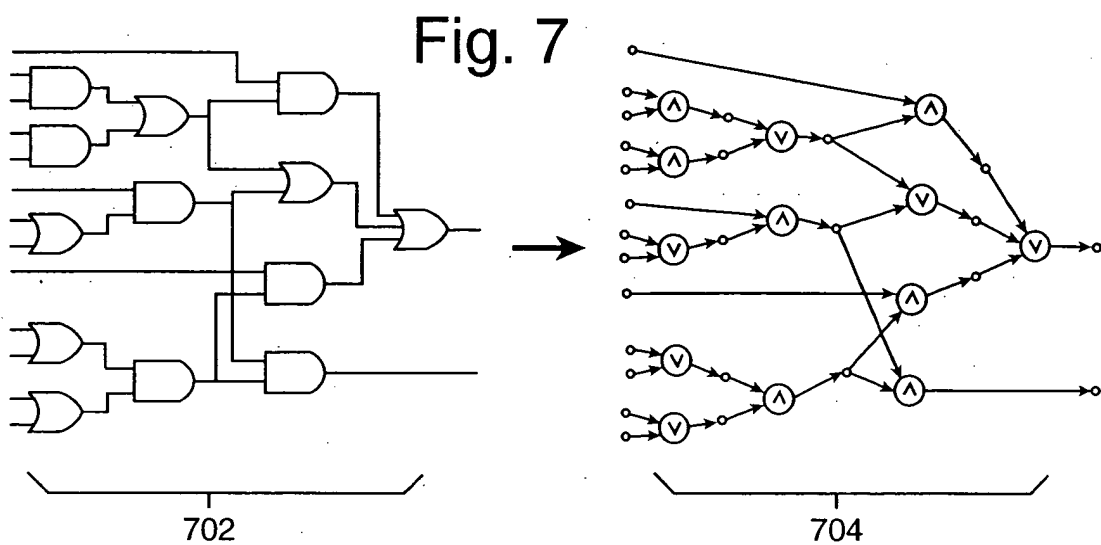
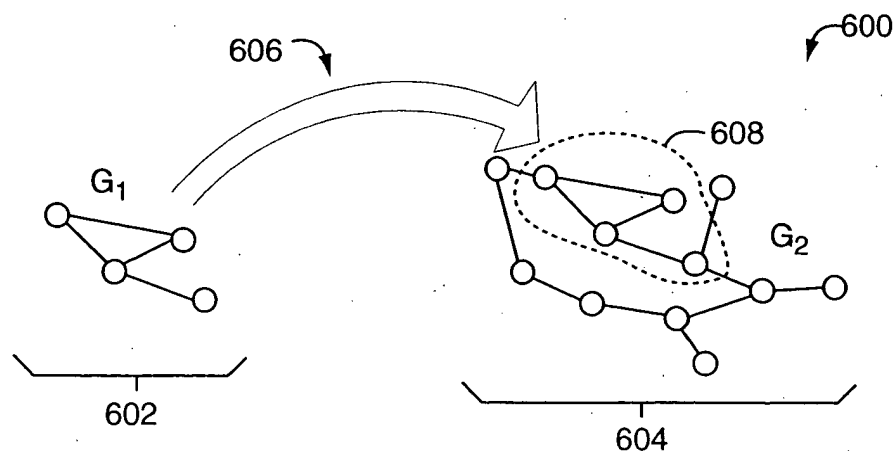


Fig. 9


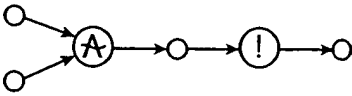
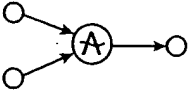
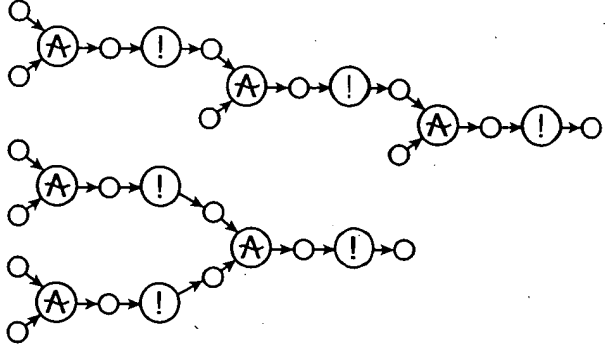
inv	! a	
and2	a b	
nand2	! (a b)	
and4	a b c d	

Fig. 10

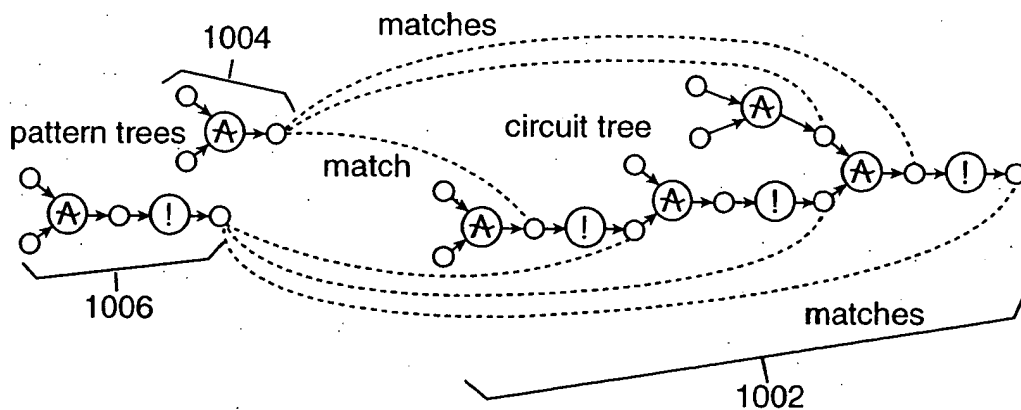


Fig. 11

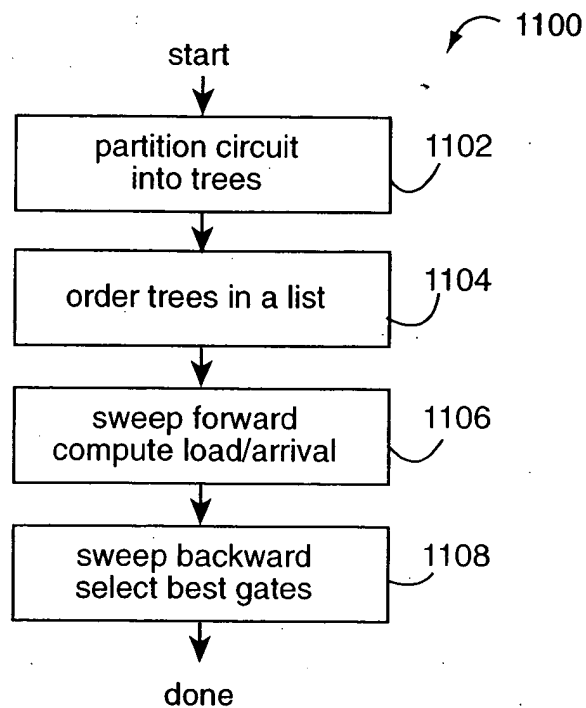
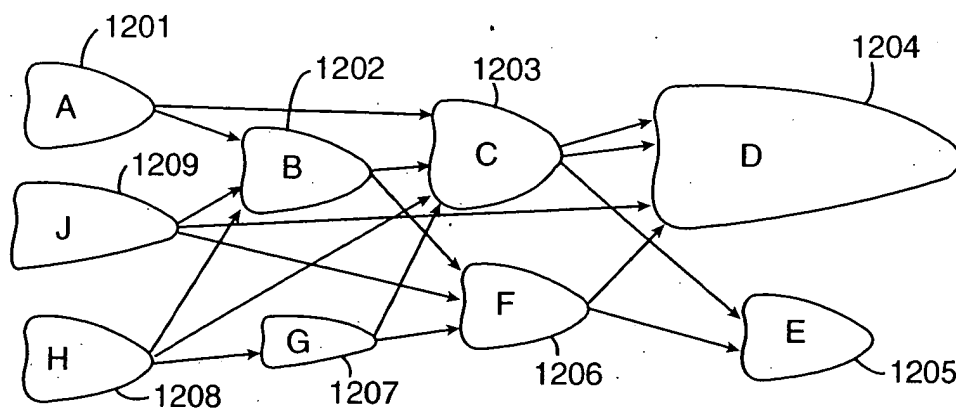


Fig. 12



1300

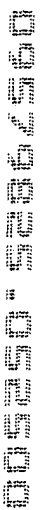


Fig. 14

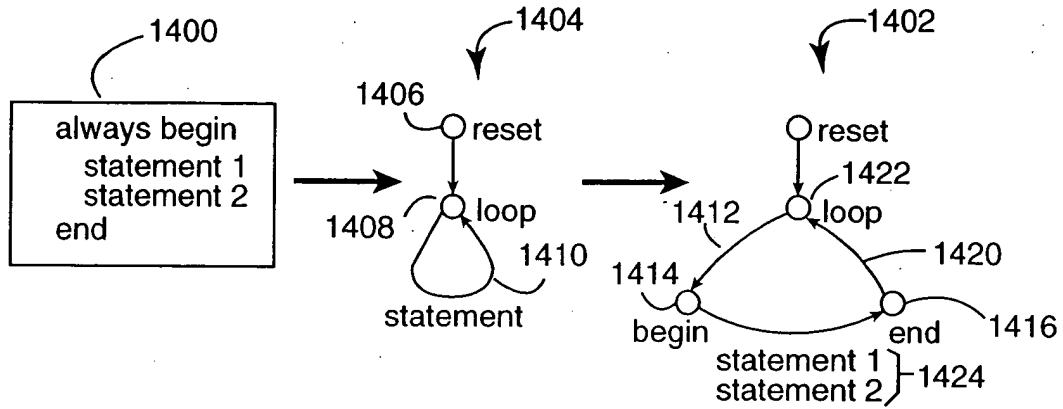


Fig. 15

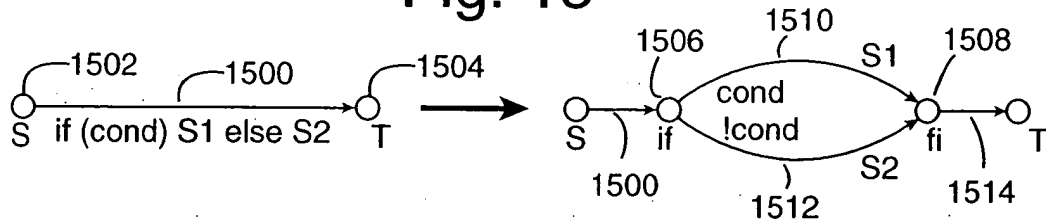


Fig. 16A



Fig. 16B

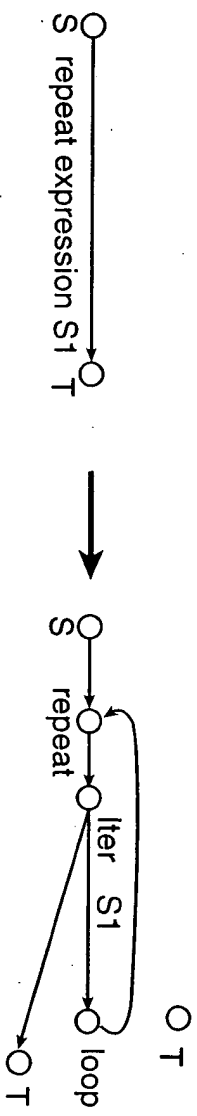


Fig. 16C

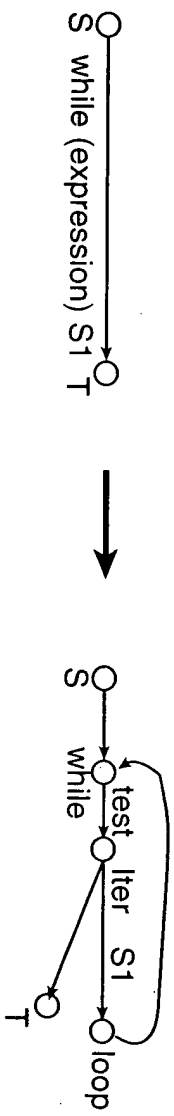


Fig. 16D

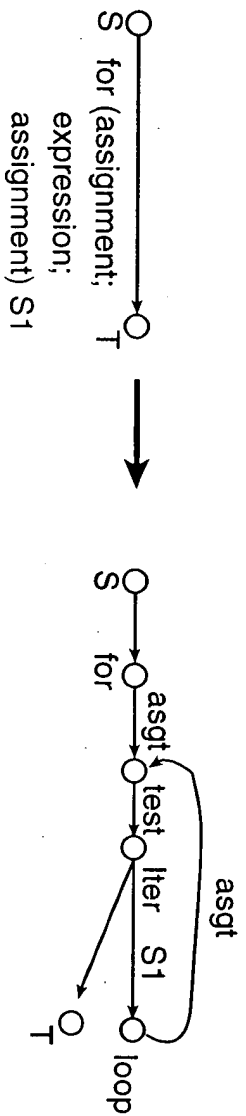


Fig. 17

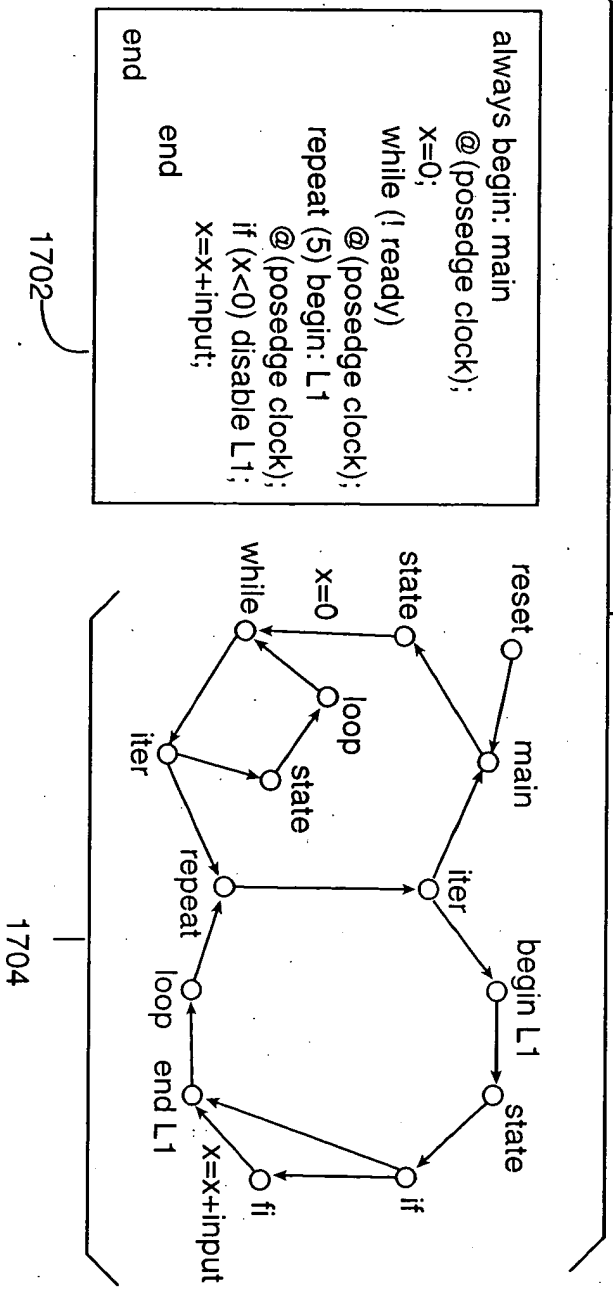


Fig. 18

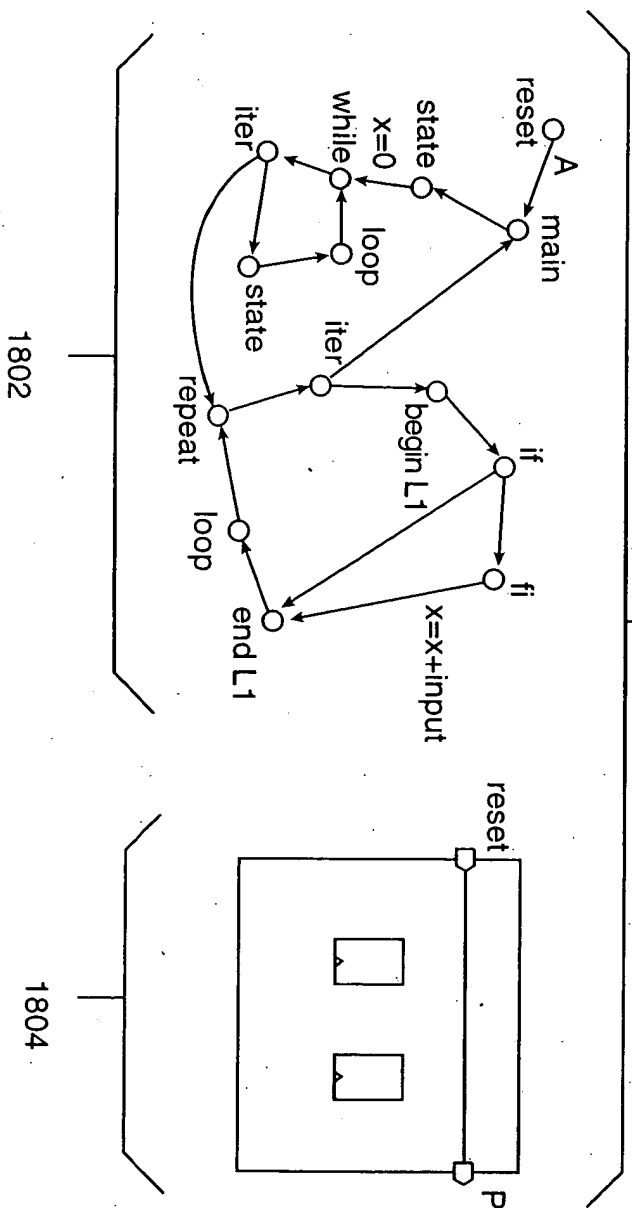


Fig. 19A

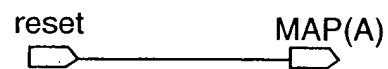
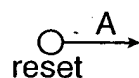


Fig. 19B

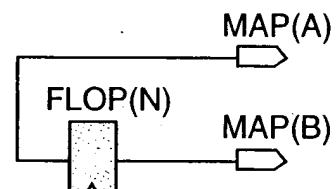
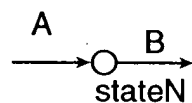


Fig. 19C

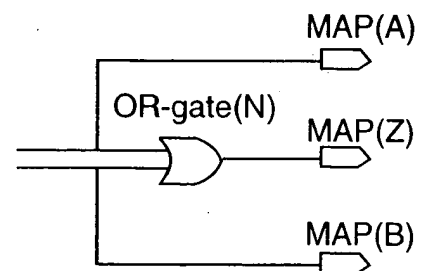
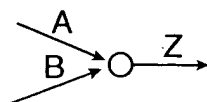


Fig. 19D

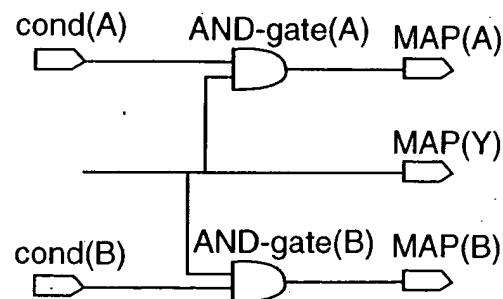
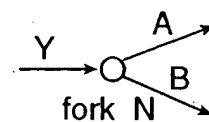
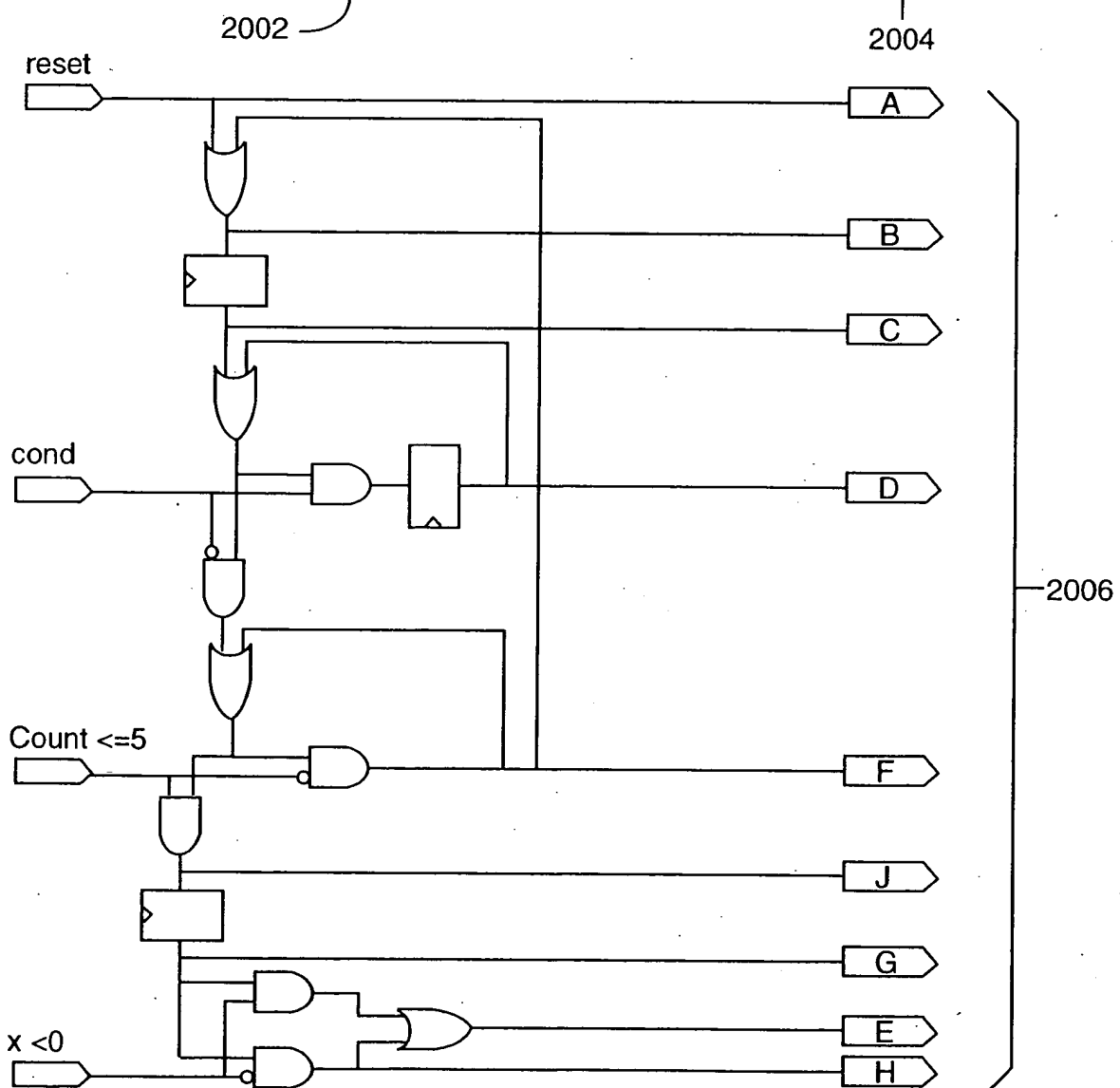
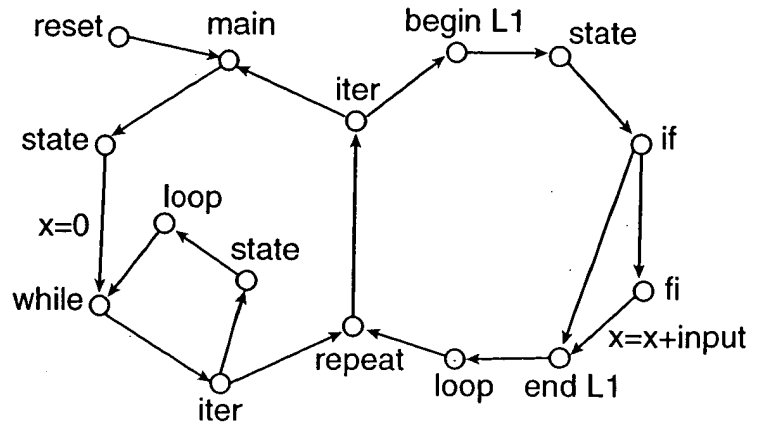


Fig. 20

```

always begin: main
  @(posedge clock);
  x=0;
  while (! ready)
    @(posedge clock);
  repeat (5) begin: L1
    @(posedge clock);
    if (x<0) disable L1;
    x=x+input;
  end
end
  
```



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